IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. **(Currently Amended)** A hardware system for performing media access control functions between a host central processing unit and a network, the system comprising:

a buffer interface that sends frames to the host central processing unit and receives frames from the host central processing unit;

a frame transmitter that includes a transmit buffer that receives frames from the buffer interface and sends frames to the network;

a frame receiver that includes a receive buffer that receives frames from the network and sends frames to the buffer interface; and

an encryption/decryption block that sends and receives frames between the transmit buffer and the receive buffer.

~~A cyclic redundancy code block that receives frames from the receive state machine and the transmit buffer and sends frames to the transmit state machine; and~~

~~a timer block that controls timing for frames that are respectively sent from and received by the system~~.

2. **(Currently Amended)** A method for processing frames from a network to a host in a media access control layer [[with hardware operations]], the [[hardware operations]] **method** comprising:

receiving an incoming frame from the network; and

processing, **using operations implemented by hardware in an integrated circuit,** the incoming frame for time-critical functions, the time critical functions[[;]] including:

sending an outgoing frame corresponding to the incoming frame to the host;

formulating time-critical responses;

accumulating statistics; and

updating a media access control state.

3. (Previously Presented) The hardware system according to claim 1 wherein the frame transmitter includes a transmit state machine, the frame receiver includes a receive state machine, and further including:

a cyclic redundancy code block that receives frames from the receive state machine and the transmit buffer and sends frames to the transmit state machine; and

a timer block that controls timing for frames that are respectively sent from and received by the system.

4. (Previously Presented) The hardware system according to claim 1 wherein the frame receiver further includes a filtering block for filtering frames.

5. (Previously Presented) The hardware system according to claim 1 wherein the frame receiver further includes a retry operations block for determining when retransmission of a particular frame is needed.

6. (Previously Presented) The hardware system according to claim 1 wherein the frame transmitter includes an acknowledgement block for determining that a particular frame was anticipated and sending an acknowledgement message corresponding thereto.

7. (Previously Presented) The hardware system according to claim 1 wherein the frame transmitter further includes a special frames generation block.

8. (Previously Presented) The hardware system according to claim 7 wherein the special frames generation block includes means for generating beacons.

9. (Previously Presented) The hardware system according to claim 1 further including a timer block that controls timing for frames that are sent from and received by the system.

10. (Previously Presented) The hardware system according to claim 9 wherein the frame transmitter includes a transmit state machine, the frame receiver includes a receive state machine, and further including:

a cyclic redundancy code block that receives frames from the receive state machine and the transmit buffer and sends frames to the transmit state machine.

11. (Previously Presented) The hardware system according to claim 9 wherein the frame receiver further includes a filtering block for filtering frames.

12. (Previously Presented) The hardware system according to claim 9 wherein the frame receiver further includes a retry operations block for determining whether retransmission of a particular frame is needed.

13. (Previously Presented) The hardware system according to claim 9 wherein the frame transmitter includes an acknowledgement block for determining that a particular frame was anticipated and sending an acknowledgement message corresponding thereto.

14. (Previously Presented) The hardware system according to claim 9 wherein the frame transmitter further includes a special frames generation block.

15. (Previously Presented) The hardware system according to claim 14 wherein the special frames generation block includes means for generating beacons.

16. (Previously Presented) A hardware system for performing media access control functions between a host central processing unit and a network, the system comprising:

a buffer interface that sends frames to the host central processing unit and receives frames from the host central processing unit;

a frame transmitter that includes a transmit buffer that receives frames from the buffer interface and sends frames to the network;

a frame receiver that includes a receive buffer that receives frames from the network and sends frames to the buffer interface; and

a timer block that controls timing for frames that are sent from and received by the system, the timer block thereby controlling interframe spacing and timing.

17. (Previously Presented) The hardware system according to claim 16 wherein the frame transmitter includes a transmit state machine, the frame receiver includes a receive state machine, and further including:

a cyclic redundancy code block that receives frames from the receive state machine and the transmit buffer and sends frames to the transmit state machine.

18. (Previously Presented) The hardware system according to claim 16 wherein the frame receiver further includes a filtering block for filtering frames.

19. (Previously Presented) The hardware system according to claim 16 wherein the frame receiver further includes a retry operations block for determining whether retransmission of a particular frame is needed.

20. (Previously Presented) The hardware system according to claim 16 wherein the frame transmitter includes an acknowledgement block for determining that a particular frame was anticipated and sending an acknowledgement message corresponding thereto.

21. (Previously Presented) The hardware system according to claim 16 wherein the frame transmitter further includes a special frames generation block.

22. (Previously Presented) The hardware system according to claim 21 wherein the special frames generation block includes means for generating beacons.

23. (Previously Presented) The hardware system according to claim 16 further including an encryption/decryption block that sends and receives frames between the transmit buffer and the receive buffer.

24. (Previously Presented) The method according to claim 2 wherein the time critical function of formulating time-critical responses includes formulating an outgoing response frame for transmission to the network.

25. (Previously Presented) The method according to claim 24 wherein the time critical function of formulating an outgoing response frame includes transmitting the outgoing response frame to the network.

26. (Previously Presented) The method according to claim 25 wherein the hardware operations for transmitting the outgoing response frame include generating a special frame.

27. (Previously Presented) The method according to claim 26 wherein the special frame includes a beacon.

28. (Previously Presented) The method according to claim 26 wherein the hardware operation of formulating an outgoing response frame includes receiving an incoming frame from the host central processing unit corresponding to the outgoing response frame.

29. (Previously Presented) The method according to claim 2 wherein the time critical functions implemented by hardware operations include decrypting the incoming frame.

30. (Previously Presented) The method according to claim 2 wherein the time critical functions implemented by hardware operations include determining whether retransmission of a particular frame is needed.

31. (Previously Presented) The method according to claim 2 wherein the time critical functions implemented by hardware operations include determining whether a particular frame was anticipated and sending an acknowledgement message corresponding thereto.

32. (New) The hardware system according to claim 1, wherein the buffer interface, frame transmitter, frame receiver and encryption/decryption block implement certain functions of a media access control (MAC) sublayer in accordance with IEEE 802.11.

33. (New) The hardware system according to claim 16, wherein the buffer interface, frame transmitter, frame receiver and timer block implement certain functions of a media access control (MAC) sublayer in accordance with IEEE 802.11.

34. (New) The method according to claim 2, wherein the time-critical functions comprise certain functions of a media access control (MAC) sublayer in accordance with IEEE 802.11.

35. (New) The hardware system according to claim 1, wherein the buffer interface, frame transmitter, frame receiver and encryption/decryption block are together comprised of a single integrated circuit.

36. (New) The hardware system according to claim 16, wherein the buffer interface, frame transmitter, frame receiver and timer block are together comprised of a single integrated circuit.

37. (New) The method according to claim 2, wherein the integrated circuit is comprised of a single integrated circuit.